

WHAT IS CLAIMED IS:

1 1. A memory cell comprising:
2 a memory device having a set of memory ports, each memory port adapted to
3 access to the memory device;
4 an address register having a plurality of sets of address lines, each set of
5 address lines adapted to communicate a memory address with one of the set of memory ports;
6 and
7 a memory partitioning set including at least one memory partitioning circuit,
8 wherein the memory partitioning circuit is connected between an address line of one of the
9 sets of address lines and a corresponding input of one of the set of memory ports, and
10 wherein the memory partitioning circuit includes a first operation mode adapted to hold the
11 corresponding input of one of the set of memory ports to a fixed value and a second operation
12 mode adapted to pass the value of the connected address line to the corresponding input of
13 one of the set of memory ports.

1 2. The memory cell of claim 1, wherein the memory partitioning set
2 further comprises:
3 a first memory partitioning circuit connected with a first address line of the
4 address register and an input of a first memory port of the memory device;
5 a second memory partitioning circuit connected with a second address line of
6 the address register and an input of a second memory port of the memory device; and
7 wherein the first and second memory partitioning circuits are adapted to hold
8 the inputs of their respective memory ports of the memory device to complementary values,
9 thereby dividing the memory device into at least two single port memory partitions.

1 3. The memory cell of claim 1, wherein at least one memory partitioning
2 circuit of the memory partitioning set includes a third operation mode adapted to invert the
3 value of an address line of one of the sets of address lines.

1 4. The memory cell of claim 1, wherein at least one of the memory
2 partitioning circuits of the memory partitioning set is responsive to a programmable device
3 configuration specifying the mode of operation of the memory partitioning circuit.

1 5. The memory cell of claim 1, wherein at least one memory partitioning
2 circuit is comprised of at least one multiplexer and an inverter gate.

1 6. The memory cell of claim 1, wherein the multiple port memory device
2 is a two port RAM device.

1 7. A programmable device comprising:
2 a plurality of logic cells each adapted to perform a logic operation specified by
3 a programmable device configuration;
4 a configuration memory adapted to store a programmable device
5 configuration; and
6 at least one memory cell comprising:
7 a memory device having a set of memory ports, each memory port adapted to
8 access to the memory device;
9 an address register having a plurality of sets of address lines, each set of
10 address lines adapted to communicate a memory address with one of the set of memory ports;
11 and
12 a memory partitioning set of at least one memory partitioning circuit
13 connected between an address line of one of the sets of address lines and a corresponding
14 input of one of the set of memory ports, wherein the memory partitioning circuit includes a
15 first operation mode adapted to hold the corresponding input of one of the set of memory
16 ports to a fixed value and a second mode of operation adapted to pass the value of the
17 connected address line to the corresponding input of one of the set of memory ports.

1 8. The programmable device of claim 7, wherein the memory partitioning
2 set further comprises:
3 a first memory partitioning circuit connected with a first address line of the
4 address register and an input of a first memory port of the memory device;
5 a second memory partitioning circuit connected with a second address line of
6 the address register and an input of a second memory port of the memory device; and
7 wherein the first and second memory partitioning circuits are adapted to hold
8 the inputs of their respective memory ports of the memory device to complementary values,
9 thereby dividing the memory device into at least two single port memory partitions.

1 9. The programmable device of claim 7, wherein at least one memory
2 partitioning circuit of the memory partitioning set includes a third operation mode adapted to
3 invert the value of an address line of one of the sets of address lines.

1 10. The programmable device of claim 7, wherein at least one of the
2 memory partitioning circuits of the memory partitioning set is responsive to a programmable
3 device configuration specifying the mode of operation of the memory partitioning circuit.

1 11. The programmable device of claim 7, wherein at least one memory
2 partitioning circuit is comprised of at least one multiplexer and an inverter gate.

1 12. The programmable device of claim 7, wherein the multiple port
2 memory device is a two port RAM device.

1 13. A system having a plurality of devices, the system comprising:
2 a non-volatile memory device storing a programmable device configuration;
3 a programmable device connected with the non-volatile memory device, the
4 programmable device comprising:
5 a plurality of logic cells each adapted to perform a logic operation specified by
6 a programmable device configuration;
7 a configuration memory adapted to store a programmable device configuration
8 received from the non-volatile memory device; and
9 at least one memory cell comprising:
10 a memory device having a set of memory ports, each memory port adapted to
11 access to the memory device;
12 an address register having a plurality of sets of address lines, each set of
13 address lines adapted to communicate a memory address with one of the set of memory ports;
14 and
15 a memory partitioning set of at least one memory partitioning circuit
16 connected between an address line of one of the sets of address lines and a corresponding
17 input of one of the set of memory ports, wherein the memory partitioning circuit includes a
18 first operation mode adapted to hold the corresponding input of one of the set of memory
19 ports to a fixed value and a second mode of operation adapted to pass the value of the
20 connected address line to the corresponding input of one of the set of memory ports.

1 14. The system of claim 13, wherein the memory partitioning set further
2 comprises:

3 a first memory partitioning circuit connected with a first address line of the
4 address register and an input of a first memory port of the memory device;

5 a second memory partitioning circuit connected with a second address line of
6 the address register and an input of a second memory port of the memory device; and

7 wherein the first and second memory partitioning circuits are adapted to hold
8 the inputs of their respective memory ports of the memory device to complementary values,
9 thereby dividing the memory device into at least two single port memory partitions.

1 15. The system of claim 13, wherein at least one memory partitioning
2 circuit of the memory partitioning set includes a third operation mode adapted to invert the
3 value of an address line of one of the sets of address lines.

1 16. The system of claim 13, wherein at least one of the memory
2 partitioning circuits of the memory partitioning set is responsive to a programmable device
3 configuration specifying the mode of operation of the memory partitioning circuit.

1 17. The system of claim 13, wherein at least one memory partitioning
2 circuit is comprised of at least one multiplexer and an inverter gate.

1 18. The system of claim 13, wherein the multiple port memory device is a
2 two port RAM device.

1 19. An information storage medium including a device configuration
2 specifying a configuration of a programmable device, the device configuration comprising:

3 a first portion adapted to configure a plurality of logic cells of a programmable
4 device to perform a plurality of logic operations;

5 a second portion adapted to configure a reconfigurable switching circuit of the
6 programmable device to selectively route data connections between the plurality of logic
7 cells; and

8 a third portion adapted to configure a set of memory partitioning circuits
9 associated with a memory cell of the programmable device, wherein each of the set of
10 memory partitioning circuits has a first operation mode adapted to hold an input of a first
11 memory port of a multiple port memory device of the memory cell to a fixed value and a

12 second operation mode adapted to pass a value of an address line to the input of a first
13 memory port of a multiple port memory device of the memory cell.

1 20. The information storage medium of claim 19, wherein the set of
2 memory partitioning circuits includes:
3 a first memory partitioning circuit connected with a first address line of the
4 address register and an input of a first memory port of the memory device; and
5 a second memory partitioning circuit connected with a second address line of
6 the address register and an input of a second memory port of the memory device;
7 and wherein the third portion of the device configuration is adapted to
8 configure the first and second memory partitioning circuits to hold the inputs of their
9 respective memory ports of the memory device to complementary values, thereby dividing
10 the multiple port memory device into at least two single port memory partitions.

1 21. The information storage medium of claim 19, wherein at least one
2 memory partitioning circuit of the set of memory partitioning circuits includes a third
3 operation mode adapted to invert the value of an address line of one of the sets of address
4 lines.

1 22. The information storage medium of claim 19, wherein at least one
2 memory partitioning circuit is comprised of at least one multiplexer and an inverter gate.

3 23. The information storage medium of claim 19, wherein the multiple
4 port memory device is a two port RAM device.